Dual, 4.5ns, Single Supply 3V/5V Comparator with Rail-to-Rail Outputs

September 1998

FEATURES

- **UltraFast: 4.5ns at 20mV Overdrive**
  7ns at 5mV Overdrive
- **Low Power: 4mA per Comparator**
- Optimized for 3V and 5V Operation
- Input Voltage Range Extends 100mV Below Negative Rail
- TTL/CMOS Compatible Rail-to-Rail Outputs
- Internal Hysteresis with Specified Limits
- Low Dynamic Current Drain; 15µA/(V-MHz), Dominated by Load In Most Circuits

APPLICATIONS

- Crystal Oscillator Circuits
- Window Comparators
- Threshold Detectors/Discriminators
- Line Receivers
- Zero-Crossing Detectors
- High Speed Sampling Circuits

DESCRIPTION

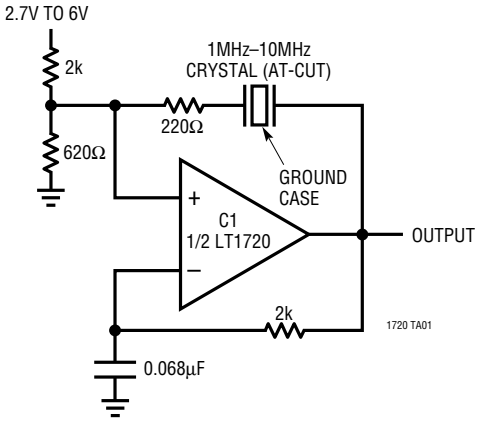
The LT®1720 is an UltraFast™ dual comparator optimized for single supply operation, with a supply voltage range of 2.7V to 6V. The input voltage range extends from 100mV below ground to 1.2V below the supply voltage. Internal hysteresis makes the LT1720 easy to use even with slow moving input signals. The rail-to-rail outputs directly interface to TTL and CMOS. Alternatively the symmetric output drive can be harnessed for analog applications or easy translation to other single supply logic levels.

The LT1720 is available in the 8-pin SO package; three pins per comparator plus power and ground. The LT1720 is ideal for systems where small size and low power are paramount.

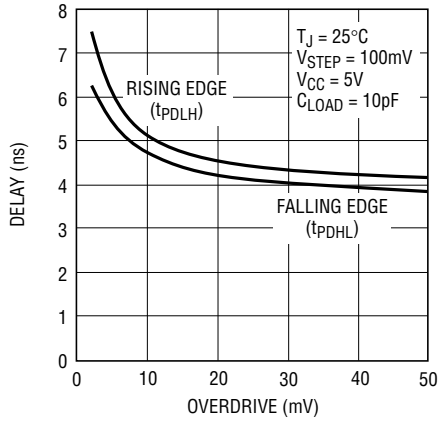
The pinout of the LT1720 minimizes parasitic effects by placing the most sensitive inputs (inverting) away from the outputs, shielded by the power rails.

TYPICAL APPLICATION

2.7V to 6V Crystal Oscillator with TTL/CMOS Output



Propagation Delay vs Overdrive

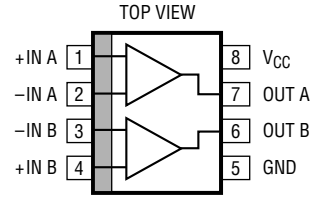


ABSOLUTE MAXIMUM RATINGS

(Note 9)

Supply Voltage, V_{CC} to GND 7V
Input Current ..... ±10mA
Output Current (Continuous) ..... ±20mA
Operating Temperature Range
C Grade ..... 0°C to 70°C
I Grade ..... –40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 200°C/W

ORDER PART NUMBER
LT1720CS8 LT1720IS8
S8 PART MARKING
1720 1720I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{CM} = 1V, C_{OUT} = 10pF, T_A = 25°C, $V_{OVERDRIVE}$ = 20mV, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage			2.7		6	V
V_{CMR}	Input Voltage Range			–0.1		V_{CC} – 1.2	V
V_{TRIP}^+ V_{TRIP}^-	Input Trip Points	(Note 1)		–2.0 –5.5		5.5 2.0	mV mV
V_{OS}	Input Offset Voltage	(Note 1)	 ●		1.0	3.0 4.5	mV mV
V_{HYST}	Input Hysteresis Voltage	(Note 1)	●	2.0	3.5	5.0	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift		●		10		µV/°C
I_B	Input Bias Current			–4		0	µA
I_{OS}	Input Offset Current					0.4	µA
CMRR	Common Mode Rejection Ratio	(Note 2)	●	55	70		dB
PSRR	Power Supply Rejection Ratio	(Note 3)	●	65	80		dB
A_V	Voltage Gain	(Note 4)			∞		
V_{OH}	Output High Voltage	I_O = –4mA, V_{IN} = V_{TRIP}^+ + 10mV	●	V_{CC} – 0.4			V
V_{OL}	Output Low Voltage	I_O = 10mA, V_{IN} = V_{TRIP}^- – 10mV	●			0.4	V
I_{CC}	Supply Current (Per Comparator)	V_{CC} = 5V	 ●		4.5	 7.0	mA mA
		V_{CC} = 3V	 ●		4	 6	mA mA
t_{PD20}	Propagation Delay	$V_{OVERDRIVE}$ = 20mV (Note 5)	 ●		4.5	6.5 8.0	ns ns
t_{PD5}	Propagation Delay	$V_{OVERDRIVE}$ = 5mV (Notes 5, 6)	 ●		7	10 13	ns ns
Δt_{PD}	Differential Propagation Delay	(Note 7) Between Channels			0.3		ns
t_{SKEW}	Propagation Delay Skew	(Note 8) Between t_{PD}^+/t_{PD}^-			1.0	1.5	ns
t_r	Output Rise Time				2.5		ns
t_f	Output Fall Time				2.2		ns

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range.

Note 1: The LT1720 comparators include internal hysteresis. The trip points are the input voltage needed to change the output state in each direction. The offset voltage is defined as the average of V_{TRIP}^+ and V_{TRIP}^-, while the hysteresis voltage is the difference of these two.

Note 2: The common mode rejection ratio is measured with V_{CC} = 5V and is defined as the change in offset voltage measured from V_{CM} = –0.1V to V_{CM} = 3.8V, divided by 3.9V.

Note 3: The power supply rejection ratio is measured with V_{CM} = 1V and is defined as the change in offset voltage measured from V_{CC} = 2.7V to V_{CC} = 6V, divided by 3.3V.

Note 4: Because of internal hysteresis, there is no small-signal region in which to measure gain. Proper operation of internal circuity is ensured by measuring V_{OH} and V_{OL} with only 10mV of overdrive.

Note 5: Propagation delay measurements made with 100mV steps. Overdrive is measured relative to $V_{TRIP}^{\pm}$.

Note 6: t_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The LT1720 is 100% tested with a 100mV step and 20mV overdrive. Correlation tests have shown that t_{PD} limits can be guaranteed with this test, if additional DC tests are performed to guarantee that all internal bias conditions are correct.

Note 7: Differential propagation delay is defined as:

$\Delta t_{PD} = |t_{PDA} - t_{PDB}|$

Note 8: Propagation Delay Skew is defined as:

$t_{SKEW} = |t_{PDLH} - t_{PDHL}|$

Note 9: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

PIN FUNCTIONS

+IN A (Pin 1): Noninverting Input of Comparator A.

–IN A (Pin 2): Inverting Input of Comparator A.

–IN B (Pin 3): Inverting Input of Comparator B.

+IN B (Pin 4): Noninverting Input of Comparator B.

GND (Pin 5): Ground.

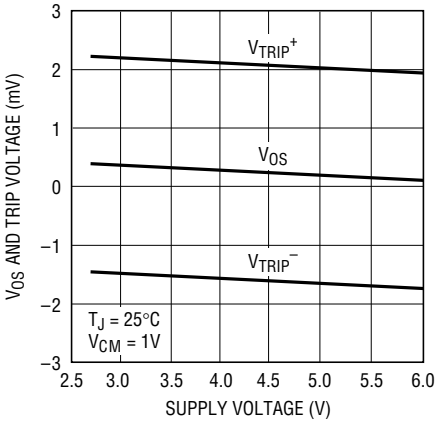
OUT B (Pin 6): Output of Comparator B.

OUT A (Pin 7): Output of Comparator A.

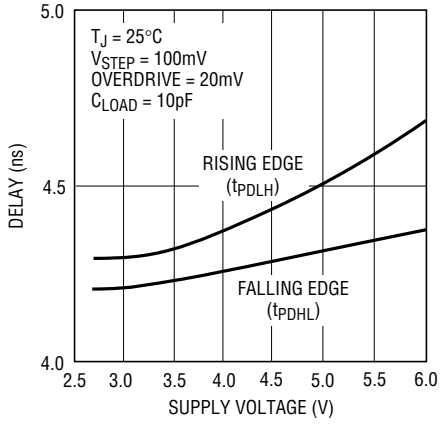
V_{CC} (Pin 8): Positive Supply Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

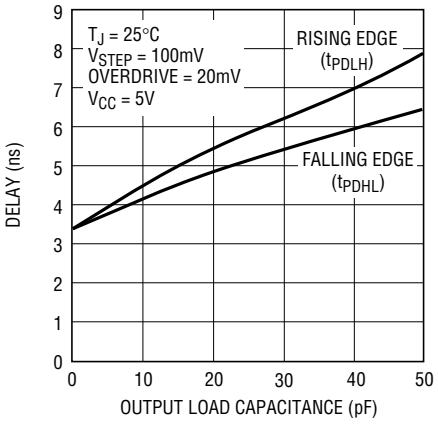
Input Offset and Trip Voltages vs Supply Voltage



Propagation Delay vs V_{CC}

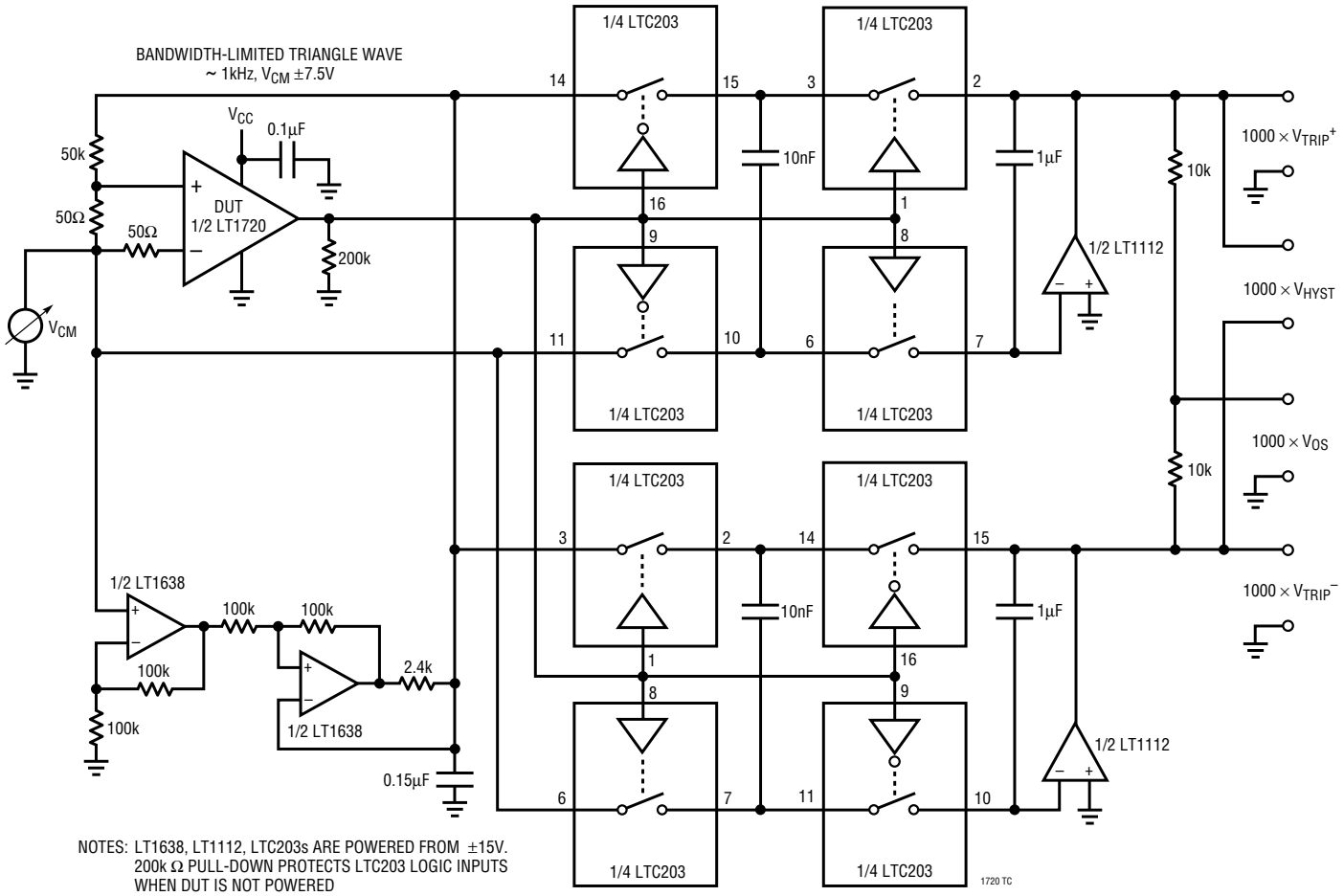


Propagation Delay vs Load Capacitance

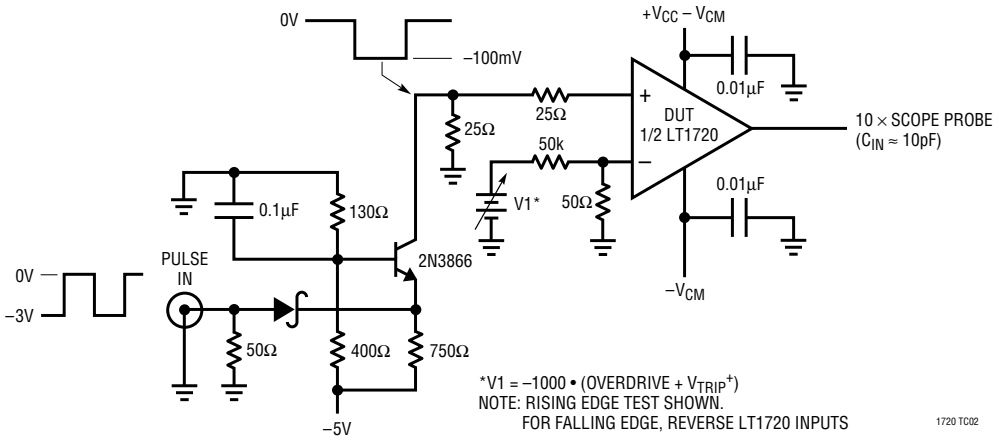


TEST CIRCUITS

$\pm V_{TRIP}$ Test Circuit



Response Time Test Circuit



APPLICATIONS INFORMATION

Input Voltage Considerations

The LT1720 is specified for a common mode range of –100mV to 3.8V when used with a single 5V supply. A more general consideration is that the common mode range is –100mV below ground to 1.2V below V_{CC}. The criterion for this common mode limit is that the output still responds correctly to a small differential input signal. Also, if one input is within the common mode limit, the other input signal can go outside the common mode limits, up to the absolute maximum limits, and the output will retain the correct polarity.

When either input signal falls below the negative common mode limit, the internal PN diode formed with the substrate can turn on, resulting in significant current flow through the die. An external Schottky clamp diode between the input and the negative rail can speed up recovery from negative overdrive by preventing the substrate diode from turning on.

When both input signals are below the negative common mode limit, phase reversal protection circuitry prevents false output inversion to at least –400mV common mode. However, the offset and hysteresis in this mode will increase dramatically, to as much as 15mV each. The input bias currents will also increase.

When both input signals are above the positive common mode limit, the input stage will get debiased and the output polarity will be random. However, the internal hysteresis will hold the output to a valid logic level, and because the biasing of the two comparators are completely independent, there will be no impact on the other comparator. When at least one of the inputs returns to within the common mode limits, recovery from this state will take as long as 1µs.

The input stage is protected against damage from large differential signals, up to and beyond a differential voltage equal to the supply voltage, limited only by the absolute maximum currents noted. The propagation delay does not increase significantly when driven with large differential voltages, but with low levels of overdrive, an apparent increase may be seen with large source resistances due to an RC delay caused by the 2pF typical input capacitance.

Input Bias Current

Input bias current is measured with both inputs held at 1V. As with any PNP differential input stage, the LT1720 bias current flows out of the device. It will go to zero on the higher of the two inputs and double on the lower of the two inputs. With more than two diode drops of differential input voltage, the LT1720's input protection circuitry activates, and current out of the lower input will increase an additional 30% and there will be a small bias current into the higher of the two input pins, of 4µA or less.

High Speed Design Considerations

Application of high speed comparators is often plagued by oscillations. The LT1720 has 4mV of internal hysteresis, which will prevent oscillations as long as parasitic output to input feedback is kept below 4mV. However, with the 2V/ns slew rate of the LT1720 outputs, a 4mV step can be created at a 100Ω input source with only 0.02pF of output to input coupling. The LT1720's pinout has been arranged to minimize problems by placing the most sensitive inputs (inverting) away from the outputs, shielded by the power rails. The input and output traces of the circuit board should also be separated, and the requisite level of isolation is readily achieved if a topside ground plane runs between the outputs and the inputs. For multilayer boards where the ground plane is internal, a topside ground or supply trace should be run between the inputs and outputs. The supply bypass should include an adjacent 0.01µF ceramic capacitor and a 2.2µF tantalum capacitor no farther than 5cm away; use more capacitance if driving more than 4mA loads. To prevent oscillations, it is helpful to balance the impedance at the inverting and noninverting inputs; source impedances should be kept low, preferably 1kΩ or less.

The outputs of the LT1720 are capable of very high slew rates. To prevent overshoot, ringing and other problems with transmission line effects, keep the output traces shorter than 10cm, or be sure to terminate the lines to maintain signal integrity. The LT1720 can drive DC terminations of 250Ω or more, but lower characteristic impedance traces can be used with series termination or AC termination topologies.

APPLICATIONS INFORMATION

Hysteresis

The LT1720 includes internal hysteresis, which makes it easier to use than other comparable speed comparators. The exact amount of hysteresis will vary from part to part as indicated in the specifications table. The hysteresis level will also vary slightly with changes in supply voltage and common mode voltage. If a comparator is used to detect a threshold crossing in one direction only, that trip point will be all that matters. Therefore, a stable offset voltage with an unpredictable level of hysteresis, as seen in many competing comparators, is useless. The LT1720 is many times better than prior comparators in these regards. In fact, the CMRR and PSRR tests are performed by checking for changes in either trip point to the limits indicated in the specifications table. Because the offset voltage is the average of the trip points, the CMRR and PSRR of the offset voltage is therefore guaranteed to be at least as good as those limits. This more stringent test also puts a limit on the common mode and power supply dependence of the hysteresis voltage.

Additional hysteresis may be added externally. The rail-to-rail outputs of the LT1720 make this more predictable than with TTL output comparators due to the LT1720's small variability of V_{OH} (output high voltage).

$\pm V_{TRIP}$ Test Circuit

The input trip points test circuit uses a 1kHz triangle wave to repeatedly trip the LT1720. The output is fed to a switched-capacitor stage that samples the slowly moving triangle wave which is fed to the LT1720 through a 1000:1 divider.

Simple Crystal Oscillator

The Crystal Oscillator shown on the front page of this data sheet operates from 2.7V to 6V with a simple AT-cut crystal from 1MHz to 10MHz using one comparator of an LT1720. As the power is applied, the circuit remains off until the LT1720 bias circuits activate, at a typical V_{CC} of 2V to 2.2V (25°C), at which point the desired frequency output is generated.

50% Duty Cycle Crystal Oscillator

If a 50% duty cycle is required, the circuit shown in Figure 1 uses the other half of the LT1720 and an op amp configured as a differential integrator to drive the duty cycle to precisely 50%. Again, the circuit operates from 2.7V to 6 V, and the skew between the edges of the two outputs are shown in Figure 2. There is a slight duty cycle dependence on comparator loading, so equal capacitive and resistive loading should be used in critical applications. Another variation of this circuit would be to create nonstandard duty cycles, either fixed or electronically variable, by adding additional fixed or variable inputs to the LT1636 input nodes through suitably scaled resistors.

Voltage-Controlled Clock Skew

A tuning voltage of 0V to 2V creates approximately ±10ns of skew between two output clocks. Refer to the circuit shown in Figure 3 which operates from 2.7V to 6V.

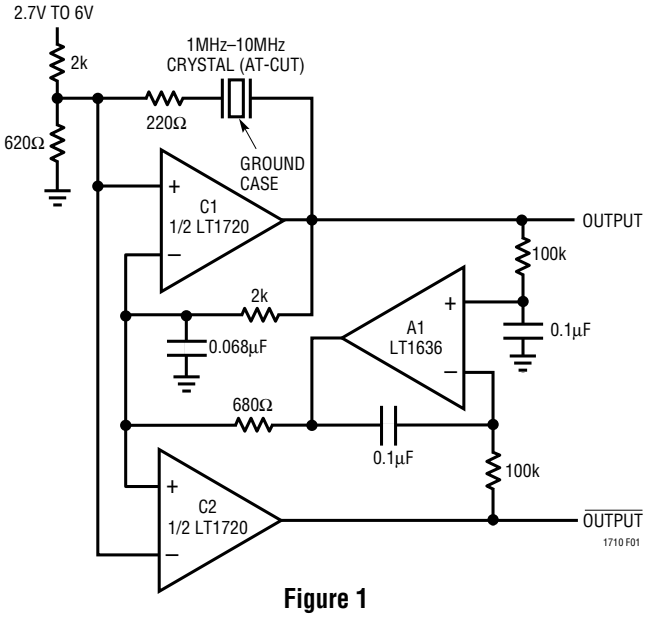


Figure 1

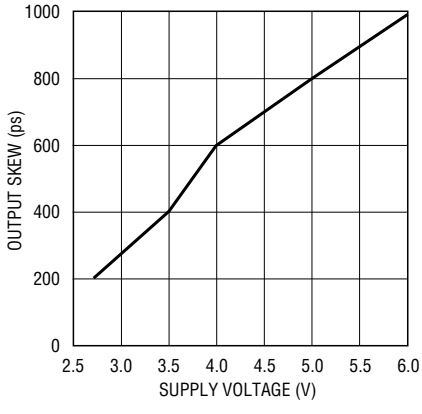
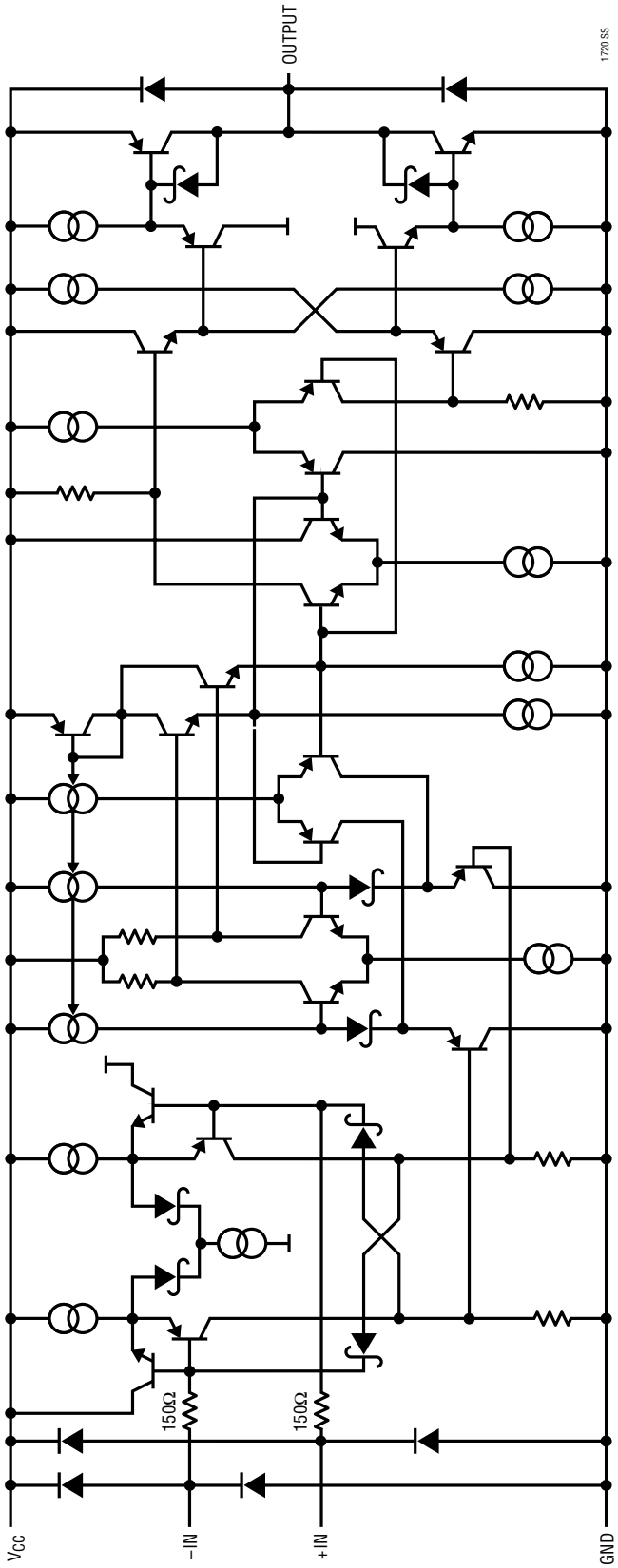


Figure 2

SIMPLIFIED SCHEMATIC



TYPICAL APPLICATION

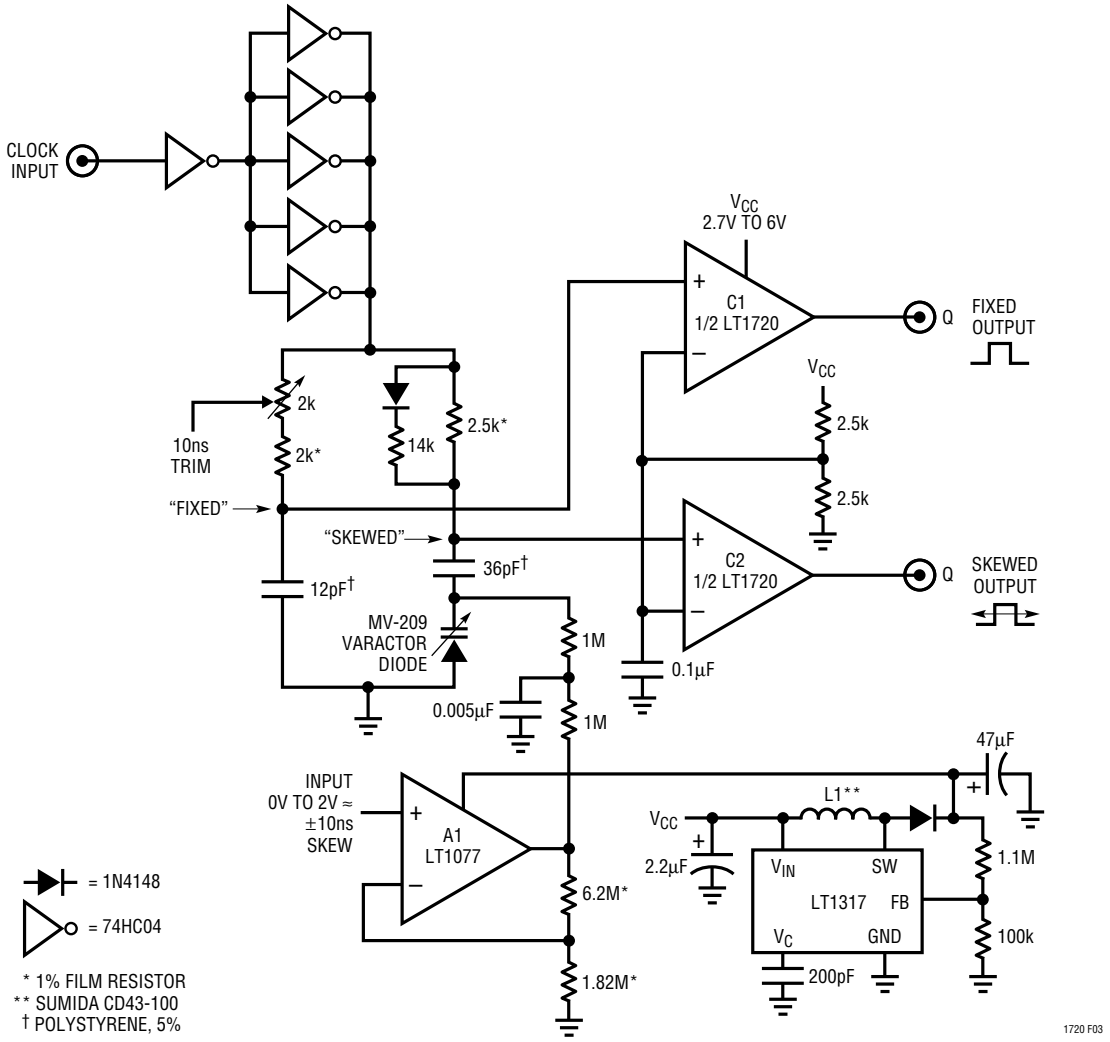


Figure 3. Voltage-Controlled Clock Skew

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1016	UltraFast Precision Comparator	Industry Standard 10ns Comparator
LT1116	12ns Single Supply Ground-Sensing Comparator	Single Supply Version of LT1016
LT1394	7ns, UltraFast, Single Supply Comparator	6mA Single Supply Comparator
LT1671	60ns, Low Power, Single Supply Comparator	450µA Single Supply Comparator

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